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PATENT
09/405,618

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In The United States Patent & Trademark Office
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Inventor(s):	Blomgren et al
Serial No.:	09/405,618
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For:	Software Modeling of Logic Signals Capable of Holding More than Two Values
Docket No.:	31876.0140
Art Unit:	2123
Examiner:	Craig, Dwin M.

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant's Reply Brief

Intrinsity, Inc. (formerly EVSX, Inc.), of Austin Texas, the real party in interest and Appellant in this appeal, files this reply to the Examiner's Answer ("Answer") mailed on 25 August 2003.

In its broadest form, the claimed invention is a signal model that models 1-of-N signals used in N-NARY logic for simulation purposes in a specific format, comprising the following elements:

(1) a signal value, said signal value further comprises the logic value of a nonbinary 1-of-N logic signal being modeled, wherein said logic value further comprises an integer greater than 1;

(2) a signal strength, said signal strength further comprises the drive state of said nonbinary 1-of-N logic signal being modeled; and

(3) a signal definition, said signal definition further comprises the defined or undefined status of said nonbinary 1-of-N logic signal being modeled.

11-14-03
Appeal Reply Brief has been noted and is forwarded to the Board of Appeals. - Dwin Craig

Other claimed embodiments include a signal model having the above features and limitations wherein the claimed logic value further comprises an integer less than or equal to 31, and a signal model having the above features and limitations wherein the claimed signal strength further comprises one of the following: the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

The Examiner originally contended the claimed embodiments, including the broadest form of the claimed invention, are anticipated under 35 USC 102(b) by *Giramma* (US Pat. No. 5,706,476), by the *IEEE Standard Multivalue Logic System for VHDL Model Interoperability* (Std_logic_1164), and by *On the Use of VHDL as a Multi-Valued Logic Simulator* by C. Rozon, IEEE 1996. In his Answer, the Examiner withdrew his rejections based on the Rozon reference, but maintained his rejections based upon the other two references. In addition, the Examiner rejected claims 1-3, 6-8, 11-13,16-18, and 21-23 as being unpatentable under the judicially created doctrine of obviousness-type double patenting in view of Leight et al., US Pat. No. 6,289,497.

The Examiner's dislike of the term of art "N-NARY" and its companion term, the "1-of-N signal" is evident throughout his Answer. Indeed, the Examiner states that if the claims language used the term "FAST14," then the claims would be "distinguished" from the prior art of record. Answer at 8. Moreover, the Examiner asserts Appellants are trying to read limitations from the specification into the claim language and not employing "means for" language to do so, but if such limitations were included in the claims, then the claims would be allowable over the prior art of record. Presumably, this refers to the use of the terms "N-NARY" and "1-of-N signal" in the claims language, and

Appellants' position that a proper interpretation of claims that use these terms of art must give full effect to them. Indeed, as demonstrated by Appellants in the initial brief, none of the references cited by the Examiner teach the claimed signal model, because none of the references teach the use or modeling of N-NARY logic or 1-of-N signals. It appears that the Examiner has come to the same conclusion, and would allow the claims if Appellants had used the term "FAST14" instead of "N-NARY" and had recited all the structure, features, and functions of N-NARY logic and 1-of-N signals in the claims.

Regarding the Examiner's FAST14-vs.-N-NARY issue, the two terms are synonymous. Intrinsity Inc., the assignee of the instant application, invented a new dynamic logic design style and family of devices and coined the term "N-NARY" to describe the logic style and the term "1-of-N signal" to describe the signal type required by and unique to N-NARY logic. Intrinsity has filed over 100 patent applications disclosing and claiming its new logic family and various N-NARY related inventions, including adders, floating point units, clock generators, registers, RAM circuits, design and testing methods and tools, etc. As of May of 2003, forty-nine of these applications had issued, and are listed in Appendix B of Appellants' Initial Brief. All of these applications and patents describe and claim Appellants' N-NARY related inventions using the defined terms "N-NARY" and "1-of-N signals."

Thereafter, Intrinsity began marketing processors and other semiconductor devices implemented in its new logic design style under the trademarks "FAST14" and "NDL," which is an acronym for "N-NARY dynamic logic." However, those skilled in the art that have followed developments in the industry and are familiar with Intrinsity's

patents are quite familiar with the original "N-NARY" term and its companion, the "1-of-N signal." Consequently, while the Examiner may dislike these terms and indeed, may have been confused by them, they are not new to this application, and substituting the term "FAST14" for the term "N-NARY" in the claims would not change the substance or scope of the claims. Moreover, since the instant application was filed long before the term "FAST14" came into existence, the term cannot be used in the claims because it is not supported or defined in the disclosure, and its meaning would not have been known to those skilled in the art at the time this application was filed.

Turning to the Examiner's contention that the structures, features, and functions of N-NARY logic and 1-of-N signals must be expressly recited in the claims (or "means for" language employed) in order to construe the claims as including those structures, features, and functions, the Examiner is wrong. N-NARY logic and 1-of-N signals are terms of art that are specifically defined in the specification. Applicants are not required to recite the entire definition of a term of art in claim language, if that term is either well known by those with skill in the art or if the term is defined in the specification. If that were the case, then the USPTO would not have developed the rather expansive set of claims interpretation rules that specifically relate to the use of defined terms in claims.

The MPEP obliges patent examiners to give claims the broadest reasonable interpretation consistent with the specification and consistent with the interpretation that those skilled in the art would reach. MPEP 2111. This means that examiners are obliged to consider every element and every limitation, and interpret words in claims as having the broadest reasonable meaning consistent with their ordinary usage, as they would be understood by one of ordinary skill in the art, *taking into account whatever*

enlightenment by way of definitions or otherwise that may be afforded by the written description contained in applicant's specification. In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997) (emphasis added). Stated another way, the words of the claim must be given their plain meaning unless the applicant has provided a clear definition in the specification. *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) ("When the applicant states the meaning that the claim terms are intended to have, the claims are examined with that meaning, in order to achieve a complete exploration of the applicant's invention and its relation to the prior art.")

An applicant may be his or her own lexicographer as long as the meaning assigned to a term is not repugnant to the term's well-known usage. MPEP 2111.01 citing *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). Any special meaning assigned to a term "must be sufficiently clear in the specification that any departure from common usage would be so understood by a person of experience in the field of the invention." *Multiform Desiccants Inc. v. Medzam Ltd.*, 133 F.3d 1473, 1477, 45 USPQ2d 1429, 1432 (Fed. Cir. 1998).

When an applicant's definition of a specific technical term clearly includes physical structures or functions, it is well-settled that the defined physical structures and functions are included as limitations in claims that incorporate the specific technical term as an element or limitation. *See Arthur A. Collins, Inc. v. Northern Telecom Ltd.*, 55 USPQ2d 1143 (Fed. Cir. 2000); *Rowe v. Dror*, 112 F.3d 473, 480, 42 USPQ2d 1550, 1555 (Fed. Cir. 1997). In *Arthur A. Collins*, a claim reciting a "time-space-time (TST) switch" limitation was held to include a 3-stage switch having certain features and

structures, as described and defined in the specification via reference to certain prior art. 55 USPQ2d 1143, 1145. Similarly, in *Rowe*, a claim reciting a "balloon angioplasty catheter" as a limitation was held to claim a catheter structure that could be inflated radially outward to dilate a narrowed region in a blood vessel, as described in the specification, and thus was not anticipated by art teaching a general purpose balloon catheter. 42 USPQ2d 1550, 1555. *See also DeMarini Sports Inc. v. Worth Inc.*, 57 USPQ2d 1889 (Fed. Cir. 2001) (bat frame is an implicit limitation in a claim directed toward an improved softball bat reciting a "large-diameter impact portion", even though claim did not include the term "frame"); *In re Lueders*, 111 F.3d 1569, 42 USPQ2d 1481 (Fed. Cir. 1997) (inherent feature not taught by prior art was clearly included in claims when claims were read in view of specification).

As this discussion demonstrates, Examiners are not free to disregard definitions in the specification when construing claims, and definitions of defined terms do not have to be recited in the claim language. In this case, the Examiner failed to follow the first rule, and is apparently unaware of the second rule. The Examiner examined the claims using his own interpretation of the term "1-of-N signal": [t]he Examiner has determined that 1-of-N signal could be interpreted as meaning 1-of-2 signals for simple binary representation, or say 1-of-3 signals for either a logic "1" or logic "2" or logic "x" where "x" is a don't care state..." Answer at 12. In addition, the Examiner asserted that "a nonbinary 1-of-N signal is <u>any</u> signal that has more than 2 possible values and that 1-of-N refers to the 1 or N possible signal representations..." Id. (emphasis in original). Neither of these two interpretations is consistent with Applicants' definition of a 1-of-N signal provided in the instant specification at page 7:

> All signals in N-nary logic are of the 1-of-N form where N is any integer greater than one. In N-nary logic, a bundle or group of N wires are used to indicate one of N possible signal values. The signal value is determined by which one of the N wires within the bundle is asserted (logical 1)....[m]ore than one wire will never be asserted for a valid 1-of-N signal. Similarly, N-nary logic generally requires that a high voltage be asserted on only one wire for all values, even 0.

Clearly, the Examiner's interpretation of a 1-of-2 signal as a binary signal conflicts with this definition: unlike a binary signal, a 1-of-2 signal used in N-NARY logic will always have 2 wires and the logic value will be dictated by which specific wire of the two wires is asserted. Binary signals travel on a single wire and the logic value is dictated by whether the wire is asserted (high voltage) or not. Likewise, the Examiner's interpretation of a 1-of-3 signal fails to account for the fact that according to Appellant's definition, a 1-of-3 signal will always have 3 wires, and the signal value will always be dictated by which one of the three wires is asserted. And, as this definition makes clear, a 1-of-N signal is not simply "any signal that has more than 2 possible values," it is a very specific signal in a very specific format having very specific constraints, and it is used only in N-NARY logic.

The claimed invention includes a signal value element that is limited to being the logic value of a nonbinary, 1-of-N signal being modeled, a signal strength element that is limited to being the drive state of the same nonbinary, 1-of-N signal being modeled, and a signal definition element that is limited to being the defined or undefined status of the same nonbinary 1-of-N signal being modeled. The Examiner is obliged to apply the above definition of a 1-of-N signal, in order to give meaning to the claim language limiting each claim element. 1-of-N signals are by definition multiwire, nonbinary signals. Means-for language is not required or appropriate.

As the Examiner has admitted, when the claims are interpreted and construed in light of the definition of a 1-of-N signal as defined in the instant specification, the claims are allowable over the prior art of record. This being the case, Appellant stands on its prior briefing addressing the Examiner's specific contentions regarding the prior art of record and the bases for the Examiner's §102 rejections, and further rebuttal concerning the Examiner's §102 rejections is not required.

Turning to the Examiner's double patenting rejection, Appellants are unsure how to make the differences between the present invention and the signal naming convention used in syntax statements to generate behavioral models and schematics any clearer. Pages 29-30 of Appellants' initial brief describe in detail how the design tool disclosed in U.S. Patent No. 6,289,497 generates behavioral models and schematics using syntax statements that include gate instantiations that include output signal variables defined according to a specific signal naming convention. The signal naming convention disclosed in the '407 patent conveys the degree, high-or-low evaluation, and clock phase of each output signal in a design. For example, the design tool of the '497 patent would be told that the output of a particular gate under design is a 1-of-4 signal (1-of-N signal degree) that evaluates on the rising edge (evaluation) of the third phase of the clock (clock phase.) In combination with the other disclosed contents of the syntax statement, the tool is provided with the information it needs to "know" in order to generate the specific logical and physical characteristics of the gate.

The '497 patent claims, in its broadest form, a syntax statement that describes the logical and physical characteristics of a logic gate, comprising a signal naming

convention and one or more gate instantiations that are built according to said signal naming convention wherein the logical and physical characteristics of the gate are described. The '497 patent describes, in detail, a syntax statement and a gate instantiation, and how each of these items fully describes the logical and physical characteristics of a gate. In contrast, there are no syntax statements in the present invention, no gate instantiations in the present invention, and the signal model of the present invention certainly does not convey any information that describes the logical and physical characteristics of a gate.

Furthermore, the Examiner is incorrect in his assertion that one of ordinary skill in the art would interpret the signal degree field claims in the '497 patent as the claimed signal strength element of the present invention. Once again, the Examiner has failed to apply Appellants' very specific definitions contained with the relevant specifications. The '497 patent very clearly defines the signal degree field in the gate instantiation as corresponding to the width of a 1-of-N signal–how many conductors the signal requires. The signal strength element of the present invention is very clearly defined to be the drive state of a 1-of-N signal, which corresponds to how strongly or weakly the one and only one conductor that is asserting the 1-of-N signal's value is driven. These are not the same thing, and one skilled in the art would understand the difference.

In view of the above, Appellant believes that the Examiner's rejection of claims 1-3, 6-8, 11-13,16-18, and 21-23 under 35 USC §102(b) was erroneous and respectfully requests that the Board reverse the Examiner's decision. In addition, Applicant believes that the Examiner's rejection of claims 1-3, 6-8, 11-13,16-18, and 21-23 as being unpatentable under the judicially created doctrine of obviousness-type double patenting

in view of Leight et al., US Pat. No. 6,289,497 was also erroneous, and respectfully requests a reversal of that decision.

Respectfully submitted,

Karen S. Wright

Date: 10/27/2003

Karen S. Wright
Reg. No. 45,240

Karen S. Wright
Matthew J. Booth
Booth & Wright, L.L.P.
PO Box 50010
Austin, Texas 78763-0010
Telephone: (512) 474-8488
Facsimile: (512) 474-7996
mailto:karen.wright@boothlaw.com
mailto:matthew.booth@boothlaw.com
http://www.boothlaw.com/

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Firm or Individual	Karen S. Wright, Reg. No. 45,240	Booth & Wright, LLP P. O. Box 50010 Austin, TX 78763-0010
Signature	Karen S. Wright	
Date	10/27/2003	

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